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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,675	12/04/2003	Koichi Hirano	2003_1690A	5709

513 7590 08/19/2005

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/726,675	HIRANO ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,17,19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,9,17,21 and 23* is/are rejected.

7)☒ Claim(s) *2-5,8,10-12,19,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Previously withdrawn from consideration as a result of a restriction requirement, 01/13/2005 now subject to being rejoined. Claims 9-12, 17, 19, 21-24 hereby rejoined and fully examined for patentability under 37 CFR 1.104. However, the claims 26-29 would be restricts based on the combination and subcombination.

2. The claims 26-27 are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the switching power supply module could be use a different capacitor than the electrolytic capacitor. The subcombination has separate utility such as the electrolytic capacitor used in a circuit other than a switching power supply module.

3. The claims 28-29 are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because a microprocessor module could be use a different capacitor other than the electrolytic capacitor. The subcombination

has separate utility such as the electrolytic capacitor used in a circuit other than the microprocessor module.

Response to Arguments

4. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 6-7, 9, 17, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,504,705) in view of Aoyama (US 6,433,417).

Regarding claim 1, Shimada et al. disclose an electrolytic capacitor (figure 8) comprising:

- a valve metal (51) element for an anode including a capacitor forming part and an electrode lead part (51A);
- a dielectric oxide film (52) provided on a surface of the valve metal element for an anode;
- a solid electrolyte layer (53) provided on the dielectric oxide film; and
- a charge collecting element/carbon layer (54) and Ag paste layer (55) for a cathode provided on the solid electrolyte layer.

Shimada et al. fail to disclose at least one through hole is formed in the electrode lead part of the valve metal element for an anode to expose a core of the valve metal element to an outside of the electrolytic capacitor.

Aoyama teaches at least one through hole (4a) is formed in the electrode lead (4) part of the valve metal element for an anode to expose a core of the valve metal element to an outside of the electrolytic capacitor (figure 5a).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the through hole anode lead of Aoyama in Shimada et al., in order to prevents the contamination from occurring, and low leakage current to be produced.

Regarding claim 6, Shimada et al. disclose at least one electrically conductive particle (56) contact with the core of the valve metal element for an anode in the electrode lead part of the valve metal element for an anode (figure 8).

Regarding claim 7, Shimada et al. further disclose at least a part of the electrically conductive particle is coated with a thermosetting resin (column 20, lines 32-36).

Regarding claim 9, Shimada et al. disclose a circuit board with a built-in capacitor (figure 9) comprising an electrolytic capacitor which is disposed within an electrically insulating layer (64) (column 17, lines 42-44), and connected to a wiring layer (63) with a conductive adhesive (figure 9), wherein the electrolytic capacitor comprising:

- a valve metal (51) element for an anode including a capacitor forming part and an electrode lead part (51A);
- a dielectric oxide film (52) provided on a surface of the valve metal element for an anode;
- a solid electrolyte layer (53) provided on the dielectric oxide film; and
- a charge collecting element/carbon layer (54) and Ag paste layer (55) for a cathode provided on the solid electrolyte layer.

Shimada et al. fail to disclose at least one through hole is formed in the electrode lead part of the valve metal element for an anode to expose a core of the valve metal element to an outside of the electrolytic capacitor.

Aoyama teaches at least one through hole (4a) is formed in the electrode lead (4) part of the valve metal element for an anode to expose a core of the valve metal element to an outside of the electrolytic capacitor (figure 5a).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the through hole anode lead of Aoyama in Shimada et al., in

order to prevents the contamination from occurring, and low leakage current to be produced.

Regarding claim 17, Shimada et al. disclose the wiring layer are disposed on both surfaces of he electrically insulating layer and are electrically connected to one another through one or more inner vias which are formed in the electrically insulating layer (figure 9).

Regarding claim 21, Shimada et al. disclose the one or more inner vias disposed so that the one or more inner vias align with the through hole formed in the electrolytic capacitor (figure 9).

Regarding claim 23, Shimada et al. further disclose a semiconductor chip (62) being electrically connected to the electrolytic capacitor disposed within the electrically insulating layer, and wherein the wiring layer is connected to an external electrode through an inner via formed in the electrically insulating layer (figure 9).

Allowable Subject Matter

7. Claims 2-5, 8, 10-12, 19, 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 2-3 and 10-11, the prior art alone or in combination does not teach the limitation of the through hole is filled with an electrically conductive resin composition containing metal powder and a thermosetting resin, and wherein the resin composition is connected to the core of the valve metal element.

With respect to claims 4-5 and 12, the prior art alone or in combination does not teach the limitation of a single electrically conductive particle or a single electrically conductive fiber is disposed within the through hole and the particle or fiber contacts with at least a part of the core of the valve metal element in the through hole.

With respect to claim 8, the prior art alone or in combination does not teach the limitation of an electrically conductive resin composition containing metal powder and a thermosetting resin is applied to a surface of the electrode lead part of the valve metal element for an anode.

With respect to claim 19, the prior art alone or in combination does not teach the limitation of the one or more inner vias are formed of a mixture of electrically conductive powder and a thermosetting resin.

With respect to claim 22, the prior art alone or in combination does not teach the limitation of the electrically conductive powder contained in a mixture that constitutes the one or more inner vias is made of the same material as that of a metal powder contained in an electrically conductive resin composition which fills the through hole formed in the electrolytic capacitor.

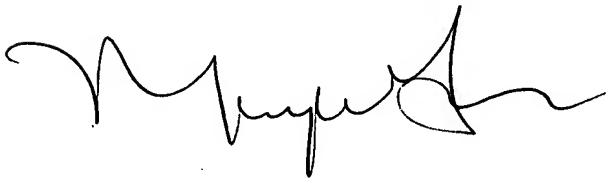
With respect to claim 24, the prior art alone or in combination does not teach the limitations of the at least one component selected from the group consisting of a semiconductor chip, another capacitor and an inductor is disposed within the electrically insulating layer within which the electrolytic capacitor is disposed or within another electrically insulating layer, and wherein the component is electrically connected to a wiring layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nguyen T. Ha
August 11, 2005